METHODS AND CIRCUITS FOR PROGRAMMABLE CURRENT LIMIT PROTECTION

Field of the Invention

[0001] The present invention relates to power converter circuits. More particularly, the present invention relates to methods and circuits for power converters having user-programmable current limit protection.

Background of the Invention

[0002] Voltage regulators, which are a type of power converter, provide an output voltage to a load within a desired range of a nominal regulated value from a voltage source that may be poorly-specified or fluctuating, or that may be at an inappropriate amplitude for the load. Such regulators may employ a switching circuit that includes one or more switching elements coupled in series or in parallel with the load. The switching elements may be, for example, power metal-oxide semiconductor field-effect transistor (MOSFET) switches.

[0003] Control circuitry regulates the output voltage and the current supplied to the load by cycling

the switch circuit between ON and OFF states. The duty cycle of the switch circuit controls the flow of power to the load, and can be varied by a variety of methods. For example, the duty cycle can be varied by (1) fixing the pulse stream frequency and varying the ON or OFF time of each pulse, (2) fixing the ON or OFF time of each pulse and varying the pulse stream frequency, or (3) a combination thereof.

[0004] To vary the ON or OFF time of each pulse or the pulse stream frequency, the control circuitry may generate a signal V_e that is proportional to the difference between the regulator's output voltage and a reference voltage. V_e may be used to provide either "voltage-mode" or "current-mode" regulation. In voltage-mode regulation, V_e and a periodic sawtooth waveform V_s may be provided as inputs to a comparator, the output of which controls the duty cycle of the switch circuit. In current-mode regulation, a voltage V_i may be generated that is proportional to the current in the output inductor, and V_i and V_e may be provided as inputs to a comparator, the output of which controls the duty cycle of the switch circuit.

[0005] Synchronous switching regulators include at least two active switching elements that typically are driven by non-overlapping drive signals to supply current at an output voltage to a load within a desired range of a nominal regulated value. Synchronous switching regulators that use power MOSFET switches frequently are used in portable battery-powered electronic products and thermally-sensitive products. These regulators convert the typically fluctuating input voltage to a regulated output voltage. Such

regulators can provide high operating efficiency and thus long battery life with little heat generation.

[0006] One fault condition that a regulator may experience is an over-current condition at the regulator output, where the current demanded by the load is significantly greater than the nominal maximum output current of the regulator. The over-current condition may cause excessive currents to flow through the components of the regulator and to be delivered at the regulator's output, causing potential damage to those components or the load, particularly when the over-current condition remains at the regulator output for a prolonged period of time.

[0007] Previous designs of switching regulators, such as the LTC1702 synchronous voltage-mode controlled buck regulator, have implemented current limit protection by comparing the drain-to-source voltage (V_{DS}) of one of the active switch elements, e.g., a MOSFET, of a synchronous switch to a reference voltage set by the user that represents the maximum allowable V_{DS} voltage. The V_{DS} voltage provides inductor current information through the relationship:

$$V_{DS} = I_L * R_{DS(ON)} \qquad \text{EQ. 1}$$

where I_L is the inductor current and $R_{DS(ON)}$ is the resistance of the MOSFET when the MOSFET is ON. Since average inductor current $I_{L,AVG}$ approximately equals the output current in a buck regulator, the inductor current flowing through the MOSFET can be used as an indicator of the output current.

[0008] The LTC1702 compares the V_{DS} voltage of the MOSFET to the user-set reference voltage with a transconductance (gm) amplifier, the output of which, averaged by an external capacitor, controls the duty

cycle of the switching regulator. When the current limit is exceeded, the duty cycle is reduced slowly until the output current is regulated at the programmed current limit. One of the problems with this approach is that there may be a delay in reducing the initial duty cycle to the lower duty cycle. During the transient phase when the duty cycle is being reduced, the inductor current is unregulated and may cause excessive currents to flow, limited only by the normally small input source, MOSFET and inductor impedances.

[0009] Other current limit schemes, such as that employed by the TPS40050 buck regulator, uses a cycle-by-cycle comparator to monitor the V_{DS} voltage of a top-side MOSFET of a synchronous switch and to instantly turn OFF the MOSFET when the V_{DS} exceeds a maximum allowable voltage. This scheme, however, also has drawbacks because the top MOSFET must be turned ON to sense the current flowing through the inductor - a situation that is undesirable during an over-current condition - and thus requires an additional fault counter and restart scheme to keep the inductor current from running away, all without ever achieving steady-state regulation of the output current (i.e., regulation of the average value of the output current).

[0010] In view of the foregoing, it would be desirable to provide methods and circuits for protecting power converters from over-current conditions by providing both steady-state and cycle-by-cycle current limit protection.

[0011] It also would be desirable to provide methods and circuits for protecting power converters from over-

current conditions, in which current limit thresholds are user-programmable.

[0012] It further would be desirable to provide methods and circuits for protecting power converters from over-current conditions, in which a signal indicative of inductor current flowing through the power converter is obtained without increasing output current, and thereby exacerbating the over-current condition.

[0013] It still further would be desirable to provide methods and circuits for protecting power converters from over-current conditions by providing cycle-by-cycle current limit protection, in which a signal indicative of inductor current flowing through the power converter is obtained without increasing output current, and thereby exacerbating the over-current condition.

Summary of the Invention

[0014] In view of the foregoing, it is an object of the present invention to provide methods and circuits for protecting power converters from over-current conditions by providing both steady-state and cycle-by-cycle current limit protection.

[0015] It also is an object of the present invention to provide methods and circuits for protecting power converters from over-current conditions, in which current limit thresholds are user-programmable.

[0016] It further is an object of the present invention to provide methods and circuits for protecting power converters from over-current conditions, in which a signal indicative of inductor current flowing through the power converter is obtained

without increasing output current, and thereby exacerbating the over-current condition.

[0017] It still further is an object of the present invention to provide methods and circuits for protecting power converters from over-current conditions by providing cycle-by-cycle current limit protection, in which a signal indicative of inductor current flowing through the power converter is obtained without increasing output current, and thereby exacerbating the over-current condition.

[0018] These and other objects of the present invention are accomplished by providing methods and circuits for protecting power converters from over-current conditions that, in a first illustrative embodiment, (1) bring average inductor current to steady-state regulation at a steady-state threshold; and (2) reduce the instantaneous inductor current after the inductor current exceeds a maximum instantaneous current threshold.

[0019] In the first illustrative embodiment, a synchronous voltage-mode switching regulator is provided having a current limit circuit that perceives the magnitude of the V_{DS} voltage of a bottom-side synchronous switch element when the switch element is ON. The magnitude of the V_{DS} voltage is proportional to the inductor current. When the magnitude of the V_{DS} voltage exceeds a user-programmable maximum V_{DS} reference threshold ($V_{MAX,REF}$) corresponding to a user-programmable steady-state current threshold, the current limit circuit slowly reduces the duty cycle of the voltage regulator until the average inductor current, and thus the output current (in buck mode), is reduced to the steady-state current threshold.

[0020] During this transient phase in which the regulator is bringing the average inductor current into steady-state regulation at the steady-state current threshold, the V_{DS} voltage also is used to provide instantaneous regulation of the instantaneous inductor current. Illustratively, the bottom-side synchronous MOSFET is kept ON in buck mode after the magnitude of the V_{DS} voltage of the bottom-side MOSFET exceeds a trip voltage threshold that corresponds to a maximum instantaneous current threshold that is greater than the steady-state current threshold. Accordingly, as the voltage regulator brings the average inductor current into steady-state regulation at the steady-state current threshold, the regulator also acts to prevent instantaneous current flowing through the regulator from reaching destructive levels.

[0021] In a second illustrative embodiment of the current limit protection circuits of the present invention, the steady-state current limit protection circuit of the first illustrative embodiment may be eliminated. Rather, a synchronous voltage-mode switching regulator may be provided, in which the bottom-side synchronous MOSFET is kept ON in buck mode after the magnitude of the V_{DS} voltage of the bottom-side MOSFET exceeds a trip voltage threshold. Accordingly, the regulator prevents instantaneous inductor current flowing through the regulator from reaching destructive levels.

[0022] The current limit circuits of the present invention may be employed in regulators of all topologies, such as buck, boost, inverting, and SEPIC, and in regulators using either voltage-mode or current-mode control.

Brief Description of the Drawings

[0023] Further features of the present invention, its nature and various advantages will be more apparent from the accompanying drawings and the following detailed description, in which:

[0024] FIG. 1A is a block diagram of an illustrative synchronous voltage regulator configured to operate in buck mode, the voltage regulator incorporating an embodiment of the current limit protection circuits of the present invention;

[0025] FIG. 1B is a block diagram of an illustrative error amplifier for use with the synchronous voltage regulator of FIG. 1A;

[0026] FIG. 1C is an alternative embodiment of the voltage regulator of FIGS. 1A-B;

[0027] FIG. 2 is a simplified schematic diagram of a an embodiment of a circuit to limit the duty cycle of the voltage regulator of FIGS. 1A-B;

[0028] FIG. 3 depicts illustrative voltage waveforms of the output and soft-start voltages of the voltage regulator of FIGS. 1A-B;

[0029] FIG. 4 shows illustrative current and voltage waveforms of the circuit of FIGS. 1A-B when the voltage regulator is operating in buck mode;

[0030] FIG. 5 is an illustrative embodiment of the synchronous voltage regulator of FIGS. 1A-B configured to operate in boost mode;

[0031] FIG. 6 shows illustrative current and voltage waveforms of the circuit of FIGS. 1A-B when the voltage regulator is operating in boost mode; and

[0032] FIG. 7 is a block diagram of a second embodiment of a synchronous voltage regulator

configured to operate in buck mode, the voltage regulator incorporating a second embodiment of a current limit protection circuit of the present invention.

Detailed Description of the Invention

[0033] Referring to FIG. 1A, an illustrative synchronous voltage regulator that operates in either buck or boost mode is described, the voltage regulator incorporating an embodiment of the current limit protection circuit of the present invention. Operation of voltage regulator 10 in buck mode is described first.

[0034] Voltage regulator 10 operates from a supply voltage V_{IN}, e.g., a battery, coupled to input terminal 14, and may be used to provide an output current at an output voltage V_{OUT} within a desired range of a nominal regulated value at output terminal 12 for driving a load (not shown), e.g., a portable laptop computer or other battery-operated system, that is coupled to the output terminal. Output voltage V_{OUT} is maintained at a regulated level by continuously and synchronously switching top-side MOSFET 16 and bottom-side MOSFET 18 of push-pull switch 20. In buck mode, top-side MOSFET 16 serves as the switch element that conducts inductor current when that current is ramping up, whereas bottom-side MOSFET 18 serves as the synchronous switch element that conducts inductor current when that current is ramping down. Push-pull switch 20 provides a supply of alternating voltage to energy storage elements - inductor 22, which conducts current in a sawtooth fashion, and output capacitor 24, which averages the sawtooth inductor current so that the load

is supplied with an output current I_{OUT} that supports load current demand at a regulated voltage.

[0035] In the voltage-mode controlled regulator of FIG. 1A, a feedback voltage (V_{FB}) proportional to the output voltage is generated at feedback pin 25 by voltage divider 26 comprising resistors R1 and R2. Voltage divider 26 is designed such that V_{FB} equals V_{REF} when output voltage V_{OUT} equals the desired nominal output voltage. When output voltage V_{OUT} is being regulated at the regulated value and there is no over-current condition at the regulator output, error amplifier 28 compares feedback voltage V_{FB} to reference voltage V_{REF}, and generates error voltage V_e. The error amplifier has a third input (to be discussed further below) which does not affect operation of the voltage regulator when output voltage V_{OUT} is being maintained at the regulated level. Error voltage V_e, stabilized by compensation circuit 31, is proportional to the difference between V_{REF} and V_{FB}, and increases as the output voltage falls.

[0036] Error voltage V_e is fed to feedforward compensation circuit 29, which adjusts the duty cycle (i.e., the percentage of time that inductor current I_L is ramping up during a single switch cycle) of switch 20 with changes in input voltage to avoid overshoot and undershoot and makes the DC loop gain independent of input voltage. With feedforward compensation circuit 29, large transient steps at the input have little effect on the output voltage. An illustrative feedforward compensation circuit is described in greater detail in U.S. Patent No. 5,055,767 by Nelson.

[0037] Feedforward compensation circuit 29 outputs a modulated error voltage ($V_{e,MOD}$), which is fed to duty

cycle limit circuit 54. To be discussed in greater detail hereinbelow, duty cycle limit circuit 54 is configured to output a signal (V_{DC}) that is the lesser of the modulated signal from the feedforward compensation circuit and a voltage indicative of that at a soft-start pin. When output voltage V_{OUT} is being regulated in steady-state operation at the regulated nominal value, duty cycle limit circuit 54 outputs the modulated signal from feedforward compensation circuit 29.

[0038] PWM comparator 30 compares signal V_{DC} to a periodic sawtooth voltage signal provided by oscillator 32 to control the duty cycle of switch 20. More specifically, when the sawtooth signal is at a level less than signal V_{DC} of the duty cycle limit circuit, PWM comparator 30 generates a logic HIGH signal that is delivered to OR gate 34, which in turn outputs a logic HIGH signal. The output of OR gate 34 is coupled to an input of AND gate 36. If the remaining non-inverted input to AND gate 36 is HIGH and the inverted inputs to AND gate 36 are LOW, AND gate 36 and drive logic gates 38 command driver 40 to turn ON top-side MOSFET 16 and driver 42 to turn OFF bottom-side MOSFET 18 so that current through inductor 22 ramps up. When the voltage of the sawtooth signal ramps up to a level greater than signal V_{DC}, PWM comparator 30 generates a logic LOW signal. Assuming the second input to OR gate 34 is also LOW, a logic LOW signal generated by PWM comparator 30 commands top-side MOSFET 16 to turn OFF and bottom-side MOSFET 18 to turn ON, ramping down inductor current I_L. Duration of the ON time of top-side MOSFET 16 is varied to maintain output voltage V_{OUT} in regulation. When the duration in which top-side

MOSFET 16 is ON increases with respect to the duration in which bottom-side MOSFET 18 is ON, the duty cycle of switch 20 increases. Thus, the duty cycle is varied to maintain output voltage V_{OUT} in regulation.

[0039] The switching frequency of push-pull switch 20 is also controlled by oscillator 32, which provides a pulsed timing signal of fixed-frequency that is the same as that of the sawtooth signal. The timing signal demarcates the beginning and end of each switch cycle by interposing logic HIGH signals between periods of logic LOW signals. Since the timing signal is supplied to an inverting input of AND gate 36, top-side MOSFET 16 is turned ON and bottom-side MOSFET 18 is turned OFF when the timing signal transitions to a logic LOW at the beginning of each switch cycle. When the timing signal transitions to a logic HIGH, the voltage regulator is commanded to turn OFF top-side MOSFET 16 and turn ON bottom-side MOSFET 18 if the remaining inputs to AND gate 36 have not already so commanded.

[0040] Voltage regulator 10 also employs a soft-start circuit that slowly increases the duty cycle of switch 20 and output voltage V_{OUT} to its regulated value when the regulator is turned ON or after a regulator-imposed shutdown. The soft-start circuit comprises external, user-programmable soft-start capacitor 44 coupled to soft-start pin 46. The voltage at soft-start pin 46 limits the maximum duty cycle of switch 20, and thus the maximum output current, and transitions the voltage regulator into shutdown when the voltage is pulled low. In alternative embodiments, soft-start capacitor 44 may be replaced with an alternative analog or digital filter. As used herein, the term "user-programmable" refers to the capability

of varying parameters of the power converter with external components or signals.

[0041] Releasing the soft-start pin allows internal current source 50 to charge soft-start capacitor 44, the internal current source 50 configured to source current in a constant or well-defined manner. As the soft-start capacitor is being charged, voltage V_{SS} at soft-start pin 46 increases responsive thereto. Soft-start voltage V_{SS} is adjusted by voltage offset 52, which reduces the soft-start voltage by a predetermined amount equal to turn-on threshold $V_{REF,ON}$ of the voltage regulator, to generate offset soft-start voltage $V_{SS,OFFSET}$. This adjustment guarantees that the signal setting the duty cycle of switch 20 is at or below a level corresponding to a 0% duty cycle when the regulator is turned ON initially. The offset soft-start voltage is fed to non-inverting input 28A of error amplifier 28, where the offset soft-start voltage further is adjusted in the error amplifier as shown in FIG. 1B to generate soft-start reference voltage $V_{SS,REF}$. In the illustrative embodiment of FIG. 1B, error amplifier 28 incorporates voltage divider 28B that reduces offset soft-start voltage $V_{SS,OFFSET}$ by one half and clamp 28C that clamps soft-start reference voltage $V_{SS,REF}$ to a minimum level that is less than reference voltage V_{REF} but greater than or equal to the voltage level at which the voltage regulator provides stable operation. Amplifier 28D then compares feedback voltage V_{FB} against the lower value of reference voltage V_{REF} or soft-start reference voltage $V_{SS,REF}$.

[0042] In an illustrative example, voltage offset 52 reduces soft-start voltage V_{SS} by 1V and reference voltage V_{REF} is 0.8V. Amplifier 28D of error amplifier

28 compares feedback voltage V_{FB} to soft-start reference voltage $V_{SS,REF}$ rather than reference voltage V_{REF} when soft-start voltage V_{SS} is less than, e.g., 2.6-3V, and outputs error voltage V_e which is proportional to the difference thereof. Offset soft-start voltage ($V_{SS,OFFSET}$) also is fed to duty cycle limit circuit 54, which outputs signal V_{DC} that is the minimum of the offset soft-start voltage and modulated error signal $V_{e,MOD}$. It will be apparent to one of ordinary skill in the art that modifications may be made to error amplifier 28 without departing from the scope of the invention.

[0043] An illustrative embodiment of duty cycle limit circuit 54 is shown in FIG. 2. Duty cycle limit circuit 54 accepts modulated error voltage $V_{e,MOD}$ from feedforward compensation circuit 29 along lead 56 and offset soft-start voltage $V_{SS,OFFSET}$ along lead 58. Modulated error voltage $V_{e,MOD}$ and offset soft-start voltage $V_{SS,OFFSET}$ are fed to respective transistors 60 and 62, which level-shift each voltage by the same predetermined amount. The lower of the two resulting voltages is supplied to the non-inverting input of PWM comparator 30, and compared to the sawtooth waveform supplied by oscillator 32 to control the duty cycle of switch 20. As illustrated in FIG. 2, transistor 64 also level shifts sawtooth waveform by the same, predetermined amount as the modulated error and soft-start voltages. Because PWM comparator 30 exhibits non-linear performance if its input voltages are below a certain level, each transistor raises the modulated error and soft-start voltages and the sawtooth waveform to bypass the non-linear range. Each transistor also

is coupled to a current source that biases the transistor to set the level-shift value.

[0044] Referring now to FIG. 3, illustrative waveforms of output voltage V_{OUT} and soft-start voltage V_{SS} for voltage regulator 10 is described. At point **A**, converter 10 comes out of shutdown when shutdown comparator 48 determines that soft-start capacitor 44 is charged to the voltage level of voltage offset 52, e.g., 1V as in the example discussed above. As soft-start capacitor 44 continues to charge, the duty cycle is gradually increased, allowing output voltage V_{OUT} to rise. Between point **A** and point **B**, control of the duty cycle shifts from soft-start voltage V_{SS} to reference voltage V_{REF} input into error amplifier 28. At point **B**, output voltage V_{OUT} has smoothly ramped to its regulated value. Thereafter, voltage regulator 10 regulates the output voltage at the regulated value. Current source 50 continues to charge soft-start capacitor 44 without influencing output voltage V_{OUT} until soft-start voltage V_{SS} is clamped at a voltage, e.g., 4V, set by transistor 66 (see FIG. 1A).

[0045] Referring back to FIG. 1A, an embodiment of the current limit protection circuit of the present invention is illustrated. Voltage regulator 10 comprises a steady-state current limit circuit that, responsive to an over-current condition at the regulator output, reduces the average current flowing through inductor 22 to a user-programmable steady-state current threshold during a transient phase and thereafter regulates average inductor current $I_{L,AVG}$ approximately at the steady-state current threshold. As is known in the art, regulation of the average inductor current at the steady-state threshold does not

necessarily mean that the average inductor current is a constant value. Rather, the current may vary to some extent. In the embodiment of FIG. 1A, the steady-state current limit circuit illustratively comprises transconductance amplifier 68 and current source 70 that is coupled to an input of the transconductance amplifier and that facilitates a user in programming the steady-state threshold.

[0046] Voltage regulator 10 also comprises a cycle-by-cycle current limit circuit that, during the transient phase, commands (1) reduction of inductor current I_L after the inductor current exceeds a maximum instantaneous threshold, and (2) escalation of inductor current I_L after the inductor current decreases below a minimum instantaneous threshold. In the embodiment of FIG. 1A, the cycle-by-cycle current limit circuit illustratively comprises hysteretic comparator 72 and voltage offset 74.

[0047] The current limit protection circuit of FIG. 1A is configured to sense the drain-to-source voltage V_{DS} of bottom-side MOSFET 18 when the bottom-side MOSFET is ON to obtain information about instantaneous inductor current I_L. Since the average inductor current approximately equals output current in a buck regulator, a signal indicative of the average difference between the V_{DS} voltage and a user-programmable reference voltage provides information about and is used to control output current. When regulator 10 is in buck mode, the V_{DS} voltage is negative with respect to ground when the bottom-side transistor is ON and output current is flowing out of output terminal 12. Inverter 76 inverts the negative

voltage to permit comparison with a positive voltage at I_{MAX} pin 80.

[0048] I_{MAX} pin 80 also is coupled to current source 70, which, along with programming resistor 78 to ground, permits a user to program a current limit reference voltage $V_{MAX,REF}$ at I_{MAX} pin 80 in a manner to be described in greater detail below. Current limit reference voltage $V_{MAX,REF}$ corresponds to the steady-state current threshold at which steady-state current limit protection initiates and to which the steady-state current limit circuit brings the average inductor current, and thus the output current (in buck mode), to steady-state regulation when the regulator experiences an over-current condition at its output.

[0049] To provide steady-state current protection, gm amplifier 68 compares the magnitude of the V_{DS} voltage of MOSFET 18 with current limit reference voltage $V_{MAX,REF}$. The output of gm amplifier 68 is coupled to user-programmable soft-start capacitor 44. When the magnitude of the V_{DS} voltage of MOSFET 18 exceeds $V_{MAX,REF}$ (i.e., inductor current I_L exceeds the steady-state current threshold) at point **C** in FIG. 3, gm amplifier 68 begins discharging soft-start capacitor 44 by sinking current proportional to the difference between the inverted V_{DS} voltage of MOSFET 18 and the current limit reference voltage $V_{MAX,REF}$ to ground, thereby reducing the voltage at soft-start pin 46. Gm amplifier 68 is configured only to sink current and not source current. When the magnitude of the V_{DS} voltage of MOSFET 18 is less than current limit reference voltage $V_{MAX,REF}$, soft-start capacitor 44 is charged by current source 50 to a maximum level set by transistor 66. Gm amplifier 68 also incorporates a clamp that

prevents the gm amplifier from pulling soft-start voltage V_{SS} below the voltage, e.g., 1V, at which voltage regulator 10 shuts down.

[0050] The voltage at soft-start pin 46 is used to control the duty cycle of switch 20 as discussed above. As gm amplifier 68 continues to sink current and thereby reduce voltage at soft-start pin 46, the decreasing soft-start voltage begins to reduce the duty cycle of switch 20 after a time delay. This permits the voltage at the soft-start pin to reduce to a level at which it resumes control of the duty cycle. As the duty cycle is reduced, so too is the average inductor and output currents. Output voltage V_{OUT} also decreases as the load discharges output capacitor 24, beginning at point **D** in FIG. 3.

[0051] Once the duty cycle is reduced to a percentage such that the average magnitude of the V_{DS} voltage approximately is equal to current limit reference voltage $V_{MAX,REF}$, i.e., the average inductor current has been reduced approximately to the steady-state current threshold, the steady-state current limit circuit regulates the average magnitude of the V_{DS} voltage approximately at the current limit reference voltage, thereby regulating the inductor current, and thus the output current in a buck regulator, approximately at the steady-state current limit threshold. More specifically, when the average magnitude of the V_{DS} voltage has decreased to the current limit reference, voltage regulator 10 regulates the duty cycle approximately at a constant percentage by (1) discharging soft-start capacitor 44 with gm amplifier 68 when the magnitude of the V_{DS} voltage rises above current limit reference voltage $V_{MAX,REF}$, and (2)

recharging the soft-start capacitor with current source 50 when the magnitude of the V_{DS} voltage decreases below the current limit reference voltage. Accordingly, when the average inductor current $I_{L,AVG}$ is in steady-state regulation at the steady-state current limit, the instantaneous inductor current I_L ripples about the steady-state current limit until the over-current condition is removed.

[0052] If the over-current condition worsens (i.e., load current demand increases) while the average inductor current, and thus the output current, is being regulated at steady-state, the average inductor and output currents increase therewith. Gm amplifier 68 again discharges soft-start capacitor 44 until the duty cycle has decreased to a percentage such that the average inductor current is reduced and brought into steady-state regulation at the steady-state current limit.

[0053] In an alternative embodiment of FIG. 1A, illustrated in FIG. 1C, current source 50 may be replaced with current sink 51 that discharges soft-start capacitor 44 in a constant or well-defined manner, while gm amplifier 68 may be configured to source current to the soft-start capacitor. During soft-start, gm amplifier 68 may be configured to slowly charge up soft-start capacitor 44 to a maximum voltage level set by an internal clamp within gm amplifier 68 or by transistor 66. When the magnitude of the V_{DS} voltage of bottom-side MOSFET 18 is less than current limit reference voltage $V_{MAX,REF}$, gm amplifier 68 may be configured to source current to the soft-start capacitor at a level to maintain the voltage across the soft-start capacitor at the maximum voltage level. If

the magnitude of the V_{DS} voltage of bottom-side MOSFET 18 increases above current limit reference voltage $V_{MAX,REF}$, gm amplifier 68 may be configured to reduce its sourced current as the magnitude of the V_{DS} voltage of the bottom-side MOSFET increases above current limit reference voltage $V_{MAX,REF}$. Since current sink 51 discharges soft-start capacitor 44 in opposition to gm amplifier 68, current sink 51 and gm amplifier 68 work in concert to regulate the voltage across soft-start capacitor 44, and thereby control the duty cycle of switch 20 as described above.

[0054] During the transient phase in which the steady-state current limit circuit is bringing the average inductor current into steady-state regulation at the steady-state current threshold, the cycle-by-cycle current limit circuit employs hysteretic comparator 72 to prevent instantaneous inductor current I_L from reaching destructive levels. Hysteretic cycle-by-cycle comparator 72 compares the magnitude of the V_{DS} voltage of MOSFET 18 with trip and untrip thresholds that are set via voltage offset 74 relative to the current limit reference voltage $V_{MAX,REF}$. While MOSFET 16 is ON, comparator 72 cannot trip, since the magnitude of the V_{DS} voltage of MOSFET 18 is not available to the current limit circuit of FIG. 1A until MOSFET 18 turns ON. Once switch 20 transitions into the OFF state, turning ON bottom-side MOSFET 18 and turning OFF top-side MOSFET 16 in buck mode, comparator 72 trips when the magnitude of the V_{DS} voltage exceeds the trip threshold, commanding top MOSFET 16 to be maintained OFF through succeeding switch cycles until the magnitude of the V_{DS} voltage has decreased below the untrip threshold. Thereafter, cycle-by-cycle

comparator 72 untrips and commands top-side MOSFET 16 to turn ON and bottom-side MOSFET 18 to turn OFF immediately independent of the clock cycle (i.e., the pulsed timing signal provided by oscillator 32). This fixes the lower limit of the instantaneous inductor current during the transient phase.

[0055] Pursuant to one aspect of the present invention, the trip and untrip thresholds of cycle-by-cycle comparator 72 are set relative to maximum reference limit $V_{MAX,REF}$ such that the average magnitude of the V_{DS} voltage during the transient phase of steady-state current protection is greater than or equal to maximum reference limit $V_{MAX,REF}$. This prevents the cycle-by-cycle comparator from interfering with the operation of the gm amplifier in reducing the duty cycle of the voltage regulator. Indeed, the untrip threshold even may be set at a voltage level greater than maximum reference limit $V_{MAX,REF}$. In the cycle-by-cycle current limit circuit of FIG. 1A, the trip and untrip thresholds are set using voltage offset 74 to offset the hysteretic band of comparator 72 relative to the programmed voltage at I_{MAX} pin 80. The trip threshold is set low enough to provide adequate instantaneous current protection during the transient phase.

[0056] To program current limit reference voltage $V_{MAX,REF}$, and thus the steady-state current threshold, a user makes a calculated or empirical selection of an appropriate value for the resistance of programming resistor 78. In particular, programming resistor 78 (R_{IMAX}) may be selected based on the following equation:

$$R_{IMAX} = V_{MAX,REF}/I_{SOURCE} \qquad \text{EQ. 2}$$

where $V_{MAX,REF}$ is the expected voltage drop across bottom MOSFET 18 at the maximum desired average inductor current and maximum junction temperature, and I_{SOURCE} is the current provided by current source 70.

[0057] For example, if R_{IMAX} is in the range between 8.3kΩ and 42kΩ and I_{SOURCE} is 12uA, the current limit circuit would bring the average inductor current into steady-state regulation at the steady-state current threshold that corresponds to an average magnitude of the V_{DS} voltage between 100mV and 500mV, respectively. The minimum value of current limit generally occurs with the largest input voltage (V_{IN}) at the highest ambient temperature, conditions that cause the largest power loss in the converter.

[0058] $V_{MAX,REF}$ may be empirically determined or calculated according to the following relationship:

$$V_{MAX,REF} = I_{LIMIT} * R_{DS(ON)} * (1+\delta) \quad \text{EQ. 3}$$

where I_{LIMIT} is the maximum desired average inductor current, $R_{DS(ON)}$ is the on-resistance of MOSFET 18, and δ is the temperature dependency of $R_{DS(ON)}$. The maximum current limit may be determined by the minimum MOSFET on-resistance. The current limit circuit of voltage regulator 10 may be disabled by floating the I_{MAX} pin.

[0059] Referring now to FIG. 4 in combination with FIG. 1A, operation of the current limit protection circuit of FIG. 1A is described. When voltage regulator 10 experiences an over-current condition at its output at time **A**, inductor current I_L continues to increase. When the inductor current exceeds the steady-state current threshold corresponding to current limit reference voltage $V_{MAX,REF}$ at time **B**, the V_{DS} voltage against which the current limit voltage

reference $V_{MAX,REF}$ is compared is unavailable. Thus, the inductor current continues to increase.

[0060] When the bottom MOSFET turns ON at time **C**, the V_{DS} voltage is available to gm amplifier 68. Since inductor current I_L is greater than the steady-state current limit, gm amplifier 68 begins to discharge soft-start capacitor 44 and sink the discharged current to ground in an amount proportional to the difference between the inductor current and the steady-state current threshold. As soft-start capacitor 44 slowly discharges, soft-start voltage V_{SS} at pin 46 decreases therewith, slowly reducing the duty cycle of the voltage regulator. Since the duty cycle has not been reduced to a low enough level to limit inductor current I_L below the steady-state current limit, inductor current I_L continues to increase.

[0061] At time **D**, the inductor current exceeds the maximum instantaneous current threshold corresponding to the trip voltage threshold. However, because bottom-side MOSFET 18 is not ON until time **E**, and thus the V_{DS} voltage is not available for comparison by cycle-by-cycle comparator 72, the inductor current continues to increase. At time **E**, switch 20 turns ON bottom-side MOSFET 18 and turns OFF top-side MOSFET 16. Cycle-by-cycle comparator 72 trips and issues a command to maintain top-side MOSFET 16 in the OFF state at the next switching cycle. Top-side transistor 16 stays OFF until time **F**, when inductor current I_L has decayed to the minimum instantaneous current threshold corresponding to the untrip voltage threshold. Cycle-by-cycle comparator 72 untrips and issues a command to turn top-side MOSFET 16 ON and bottom-side MOSFET 18 OFF. Thereafter, cycle-by-cycle comparator 72 trips

and untrips for a number of cycles until time **G** when gm amplifier 68 has reduced the duty cycle of the voltage regulator low enough to keep the average inductor current, and thus output current I_{OUT} (in a buck regulator), at the user-programmable steady-state current threshold corresponding to current limit reference voltage $V_{MAX,REF}$. At this point, the duty cycle has been reduced low enough so that cycle-by-cycle comparator 72 no longer trips and the steady-state current limit circuit regulates the inductor current in steady-state regulation approximately at the steady-state current threshold.

[0062] Once the over-current condition is removed from the output of the voltage regulator, the feedback loop reduces inductor current I_L below the steady-state current threshold. Consequently, gm amplifier 68 stops discharging soft-start capacitor 44, which is recharged by current source 50 so that the voltage regulator can regulate output voltage V_{OUT} at the desired nominal output voltage.

[0063] Voltage regulator 10 also comprises other features that are not described in detail herein. For example, voltage regulator 10 comprises circuits to enable undervoltage lockout that shuts down the regulator when the power supply is less than a predetermined threshold, pulse skip mode to increase efficiency at light loads, reverse current detection, over-temperature detection that shuts down the voltage regulator responsive to an excessive temperature, and MAX and MIN comparators that ensure that the output voltage does not exceed or decrease below the desired nominal output voltage by a particular range. Of course, additional circuits may be included or

modifications may be made based on the needs of the user application.

[0064] Referring now to FIGS. 1 and 5, voltage converter 10 of the present invention also may be employed as a boost converter. When INV pin 82 is grounded, voltage converter 10 operates in buck mode in a manner described in detail above. However, when INV pin 82 is pulled up by a predetermined voltage, e.g., 2V, voltage converter 10 operates in boost mode, wherein bottom-side MOSFET 18 acts as the switch element that conducts inductor current when that current is ramping up and top-side MOSFET 16 acts as the switch element that conducts inductor current when that current is ramping down. As illustrated in FIG. 5, input voltage V_{IN} is coupled to input terminal 14, which is disposed in series with inductor 22, whereas top-side MOSFET 16 is coupled to output capacitor 24, which delivers output current I_{OUT} to a load that may be coupled thereto.

[0065] Operation of voltage regulator 10 in boost mode is similar to that described above for buck mode operation with some exceptions. First, when the voltage regulator is in boost mode, pulse skip mode and feedforward compensation are disabled.

[0066] In boost mode, the average inductor current does not approximately equal the output current. Rather, average inductor current $I_{L,AVG}$ is a function of both duty cycle and output current I_{OUT} according to the following relationship:

$$I_{L,AVG} = I_{OUT}/(1-D) \qquad \text{EQ. 4}$$

where D is the duty cycle. In a boost converter, the duty cycle may be determined by the following relationship:

$$D = (V_{OUT}-V_{IN})/V_{OUT} \qquad \text{EQ. 5}$$

In order to ensure that the current limit circuit does not initiate at loads less than the maximum desired current, R_{IMAX} should be programmed at maximum expected duty cycle (minimum V_{IN}). This relationship should be taken into account when calculating an appropriate value for the resistance of programming resistor 78 in boost mode pursuant to EQS. 2 and 3 given above.

[0067] In boost mode, the current limit circuit of voltage converter 10 is configured to measure the inductor current by sensing the V_{DS} voltage of bottom-side MOSFET 18 when MOSFET 18 is ON. This arrangement allows for easy implementation. However, in a boost converter, the V_{DS} voltage across the bottom-side MOSFET is positive. Accordingly, inverter 76 is disabled to permit comparison against a positive voltage at I_{MAX} pin 80. Furthermore, because the V_{DS} voltage of bottom-side MOSFET 18 immediately is available to cycle-by-cycle comparator 72 when the inductor current increases to the maximum instantaneous current threshold, the cycle-by-cycle comparator trips immediately at time **E'** in FIG. 6, turning OFF bottom-side MOSFET 18 and turning ON top-side MOSFET 16, thereby permitting inductor current I_L to decrease. In contrast, when voltage regulator 10 operates in buck mode, comparator 72 delays comparator trip to time **E** in FIG. 4 when bottom-side MOSFET 18 turns ON and its V_{DS} voltage becomes available to the comparator.

[0068] Furthermore, because the V_{DS} voltage of bottom-side MOSFET 18 is unavailable to cycle-by-cycle comparator 72 when inductor current I_L decreases, voltage regulator 10 is designed to turn ON bottom-side MOSFET 18 and turn OFF top-side MOSFET 16 (at time $\mathbf{F_1}'$

in FIG. 6) three switch cycles after the cycle-by-cycle comparator trips. It does that so that cycle-by-cycle comparator 72 can access the V_{DS} voltage of bottom-side MOSFET 18 to determine whether inductor current I_L has decreased to a value less than the minimum instantaneous threshold. If the inductor current has decreased to a value less than the minimum instantaneous threshold at the end of the third switch cycle (e.g., at time $\mathbf{F_2'}$), cycle-by-cycle comparator 72 untrips and permits voltage regulator 10 to operate normally until the inductor current once again reaches the maximum instantaneous threshold, at which time the cycle-by-cycle comparator trips again.

[0069] However, if the inductor current has not decreased to a value less than the minimum instantaneous threshold, voltage regulator 10 repeats the above-described process until the inductor current has decreased to a value less than the minimum instantaneous threshold. More specifically, after the bottom-side MOSFET is turned OFF and the top-side MOSFET is turned ON at the end of the present switch cycle at time **F"**, voltage regulator 10 maintains bottom-side MOSFET 18 OFF and top-side MOSFET 16 ON for another three switch cycles. At the end of the third switch cycle, bottom-side MOSFET 18 is turned ON and top-side MOSFET 16 is turned OFF so that cycle-by-cycle comparator 72 can access the V_{DS} voltage of bottom-side MOSFET 18 to determine whether inductor current I_L has decreased to a value less than the minimum instantaneous threshold. In contrast, when voltage regulator 10 operates in buck mode, comparator 72 immediately untrips at time **F** in FIG. 4 since the V_{DS}

voltage of MOSFET 18 immediately is available to comparator 72 at that time.

[0070] In a dedicated boost regulator, the current limit circuit of the present invention may be configured to sense the V_{DS} voltage of the synchronous switch element during its ON time.

[0071] In boost mode, voltage regulator 10 provides current limit protection for "soft" shorts (i.e., when output voltage V_{OUT} is greater than input voltage V_{IN}) because, when output voltage V_{OUT} is less than input voltage V_{IN}, there is no reversal of polarity across inductor 22. For "hard" shorts, the inductor current is limited by the input supply capability and the series impedances of the inductor and the MOSFETs.

[0072] Referring now to FIG. 7, a second embodiment of a current limit protection circuit of the present invention is depicted, in which voltage regulator 90 may be configured to operate in either buck or boost mode. Voltage regulator 90 is similar to voltage regulator 10 of FIGS. 1A-B and 5, except that the steady-state current limit protection circuit incorporated in voltage regulator 10 is eliminated. To protect against over-current conditions, voltage regulator 90 includes hysteretic comparator 92, which compares the magnitude of the V_{DS} voltage of bottom-side MOSFET 18 with trip and untrip thresholds set by the hysteresis of hysteretic comparator 92 relative to a user-programmable current limit threshold. The current limit threshold is set by user-programmable resistor 94 coupled via I_{MAX} pin 96 to current source 98 in a manner similar to that described above. Furthermore, because the steady-state current limit protection circuit is eliminated in voltage regulator 90, voltage offset 74

(see FIG. 1A) also may be eliminated. The cycle-by-cycle current limit circuit of FIG. 7 operates in a manner similar to that described above with respect to the cycle-by-cycle current limit circuit of FIGS. 1A-B and 5.

[0073] Although illustrative embodiments of the present invention are described above, it will be apparent to one skilled in the art that various changes and modifications may be made without departing from the invention. For example, while the above-described embodiment measured inductor current by sensing the V_{DS} voltage of a switch element during its ON time, the current limit circuit of the present invention also may perceive inductor current by sensing the voltage drop across a resistive current shunt disposed in series with inductor 22 or across a transistor coupled in parallel with one of the switch elements. Alternative embodiments of current sensors also may be employed, such as current transformers, Hall effect devices, optical current sensors, or current mirrors.

[0074] Furthermore, while gm amplifier 68 of voltage regulator 10 of FIG. 1A is coupled to and discharges soft-start capacitor 44, soft-start capacitor 44 may be replaced by a different analog or digital filter or the gm amplifier instead may be coupled to and discharge a user-programmable or internal filter dedicated to over-current protection. This permits a voltage regulator incorporating the current limit circuits of the present invention to use alternative soft-start schemes.

[0075] In alternative embodiments of the cycle-by-cycle current limit circuit of FIGS. 1A-B, 5 and 7, hysteretic comparator 72 or 92 may be replaced by two separate comparators - a first comparator that commands

top-side MOSFET 16 to be kept OFF after the magnitude of the V_{DS} voltage of bottom-side MOSFET 18 exceeds the trip threshold, and a second comparator that commands top-side MOSFET 16 to be turned ON and bottom-side MOSFET 18 to be turned OFF after the magnitude of the V_{DS} voltage decreases below the untrip threshold in buck mode or after three switch cycles in boost mode. Furthermore, rather than untripping the cycle-by-cycle comparator after instantaneous inductor current I_L decreases below a minimum instantaneous threshold, voltage regulators 10 and 90 also may be configured to untrip the cycle-by-cycle comparator after a predetermined amount of time or number of switch cycles.

[0076] In addition, while the above-described embodiments depict the use of synchronous switches, each having two active switching elements (e.g., two MOSFETs) that are driven out of phase to supply current at a regulated voltage to a load, one of ordinary skill in the relevant art would appreciate that one of the two MOSFETs may be replaced with a passive switch element, such as a switching diode, depending on the mode of operation. The present invention also may be integrated with voltage regulators employing other types of switches having, e.g., a pair of N-MOSFETS, a pair of P-MOSFETS, one or more bipolar junction transistors or insulated gate bipolar transistors.

[0077] It will be apparent to one of ordinary skill in the art that the cycle-by-cycle current limit circuit of the present invention may be configured to turn the top-side switch element ON and the bottom-side switch element OFF at a predetermined time after the inductor current exceeds the maximum instantaneous

current threshold in buck mode, rather than waiting for the inductor current to decrease to the minimum instantaneous current threshold. Likewise, the cycle-by-cycle current limit circuit of the present invention may be configured to turn the bottom-side switch element ON and the top-side switch element OFF at a predetermined time after the inductor current exceeds the maximum instantaneous current threshold in boost mode.

[0078] Furthermore, while the above-described embodiment incorporates voltage-mode regulation of the converter's duty cycle, it should be obvious to one of ordinary skill in the art that the current limit circuit of the present invention also may be integrated with power converters having current-mode regulation. The current limit circuit of the present invention also may be integrated with alternative topologies, such as inverting and SEPIC regulators.

[0079] All reference voltages defining the predetermined thresholds may comprise the same threshold levels or one or more different levels, and may be constant or variable in nature. All current and voltage values provided herein are for illustrative purposes only, unless otherwise stated. Other values may be employed based on design choice.

[0080] It is intended in the appended claims to cover all such changes and modifications that fall within the true spirit and scope of the invention.